EV CHARGER

SOFTWARE REQUIREMENTS SPECIFICATION PHASE 1

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Revision History

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EV Charger -0100	15 June 2000	Original release.

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1. Introduction

This is the Software Requirements Specification (SRS) for the EV Charger project.

1.1 Purpose

The purpose of this SRS is to specify the requirements for development of the software to control the operation of a battery charger for an electric vehicle

1.2 Scope

This document shall contain all the requirements for the EV Charger software phase 1.

1.3 Definitions, acronyms, and abbreviations

EV Electric Vehicle
SRS Software Requirements Specification

1.4 References

The following documents form a part of this specification to the extent specified. In the case of conflict between a cited document and this specification, this specification shall be considered a superseding document.

Data Sheets

Maxim MAX110/MAX111 19-0283 Rev 3 3/96 data sheet
Intel 8752 Manual

2. Overall description

This section describes general factors that affect the product and its requirements. Items presented in these subparagraphs are **not** requirements but provide **background information** for the requirements specified in section 3.

2.1 Product perspective

This document describes the software for the phase one charging system. Phase one is an open loop control model, phase 2 will have voltage and current feedback to support several charging profiles.

2.2 Product functions

The EV Controller Software shall perform the following:

Phase One Open Loop

The unit will display the percentage of maxium on time
The up button will increase the percentage of on time
The down button will decrease the percentage of off time
Turn on the SCRs after a define period of time

2.3 User characteristics

None.

2.4 Constraints

The platform for this software is an 8752 base processor board running on an 11.05 MHz clock. The code is to be written in "C".

3. Specific requirements

The following paragraphs specify the software requirements of the EV Charger in sufficient detail to enable designers to design the system to satisfy these requirements, and testers to validate that the designed system satisfies the requirements.

3.1 External interface requirements

3.1.1 User interfaces

3.1.1.1 LCD Display

The LCD shall display % On time, battery current, battery voltage, and battery charge.

3.1.1.2 Up Button

Increases the value of the current mode

3.1.1.3 Down Button

decreases the value of the current mode

3.1.1.4 Function Button

Not used (For phase 2)

3.1.1.5 LED

An LED is provide for debugging purposes and as an indicator that the processor is running normally. During normal operation the LED should blink at a ~2-second rate

3.1.2 Hardware interfaces

3.1.2.1 LCD

The LCD uses the standard LCD 14-pin interface and command set
Data is on port 0
Control lines are on port 2
Data/Reg bit 3
Enable bit 2
R/W bit 1

3.1.2.2 RS-232

The RS-232 interface provides a communications path to collect data from the controller. It shall report %modulation, battery voltage, battery current, battery state of charge, abs pedal position and current limit status.

The RS-232 hardware is internal to the 8752 see its data sheet for more information

3.1.2.3 Trigger

the trigger output is used to turn on the SCRs.

3.1.2.4 LED

The LED is connect to port 2 bit 0 of the 8751

3.1.2.5 Switches

TBD

3.1.3 Software interfaces

None

3.1.4 Communications interfaces

RS232 Port – Transmit only no handshaking, 9600baud, N, 1
It shall report %modulation, battery voltage, battery current, battery state of charge, abs pedal position and current limit status. The data shall be in ASCI format and comma delimited. Each data packet shall end in a carriage return and line feed.

3.2 Functional requirements

3.2.1 Function SCR Triggering

The following paragraphs define the processing associated with the SCR Triggering.

3.2.1.1 Introduction

The SCRs need to be triggered at the proper point of the 60Hz phase. For 0% the SCRs shall not be triggered and at 100% the SCRs shall be triggered with out delay.

3.2.1.2 Inputs

zero crossing interrupt

3.2.1.3 Processing

When the zero crossing interrupt occurs a timer will be loaded with the current value of the phase delay time.

3.2.1.4 Outputs

SCR trigger.

3.2.2 Function Open Loop Control Phase 1

3.2.2.1 Introduction

The up and down buttons control the value of the phase delay

3.2.2.2 Inputs

Up Button
Down Button

3.2.2.3 Processing

The up button will decrease the phase delay

The Down Button will decrease the phase delay

3.2.2.4 Outputs

none

4. Qualification provisions

Section	Requirement	Qualification
3.1.2.1	LCD Display	Demonstration
3.1.1.2	Up Button	Demonstration
3.1.1.3	Down Button	Demonstration
3.1.2.2	RS-232	Demonstration
3.1.2.3	Trigger	Test
3.1.2.4	LED	Demonstration
3.2.1	SCR trigger	Test
3.2.2	Open Loop Control Phase 1	Test

5. Appendices

I/O MAP

PORT	BIT	Function
0	0	i/o Bit 0 of the LCD data/reg input
	1	i/o Bit 1 of the LCD data/reg input
	2	i/o Bit 2 of the LCD data/reg input
	3	i/o Bit 3 of the LCD data/reg input
	4	i/o Bit 4 of the LCD data/reg input
	5	i/o Bit 5 of the LCD data/reg input
	6	i/o Bit 6 of the LCD data/reg input
	7	i/o Bit 7 of the LCD data/reg input
1	0	
	1	input from the AtoD data (phase 2)
	2	
	3	
	4	
	5	Up Switch
	6	Down Switch
	7	Function Switch
2	0	Output LED
	1	Output LCD R/W
	2	Output LCD select
	3	Output LCD data/reg
	4	Output AtoD clock(phase 2)
	5	Output AtoD Select(phase 2)
	6	Output AtoD data(phase 2)
	7	SCR Trigger
Int		zero crossing